voltages with different levels are generated corresponding to a mode control signal by a bias voltage supply circuit comprising PMOS transistors P2 and P3 which have different voltages applied to the respective sources and the mode control signal input to the gates. The generated bias voltages are supplied to the n-wells of PMOS transistors. During operation, a bias voltage that is almost the same as the operation voltage is applied to the n-wells of PMOS transistors. During standby, a bias voltage higher than the operation voltage is supplied to the aforementioned n-wells of PMOS transistors. In this way, the driving currents of the transistors can be kept at a high level during operation, while leakage currents of the transistors can be restrained during standby. Consequently, high speed and low power consumption can be realized.--

A1 cont'd